UG-9696HDDAF11

Evaluation Kit User Guide

Writer:

Email:

Version: Preliminary

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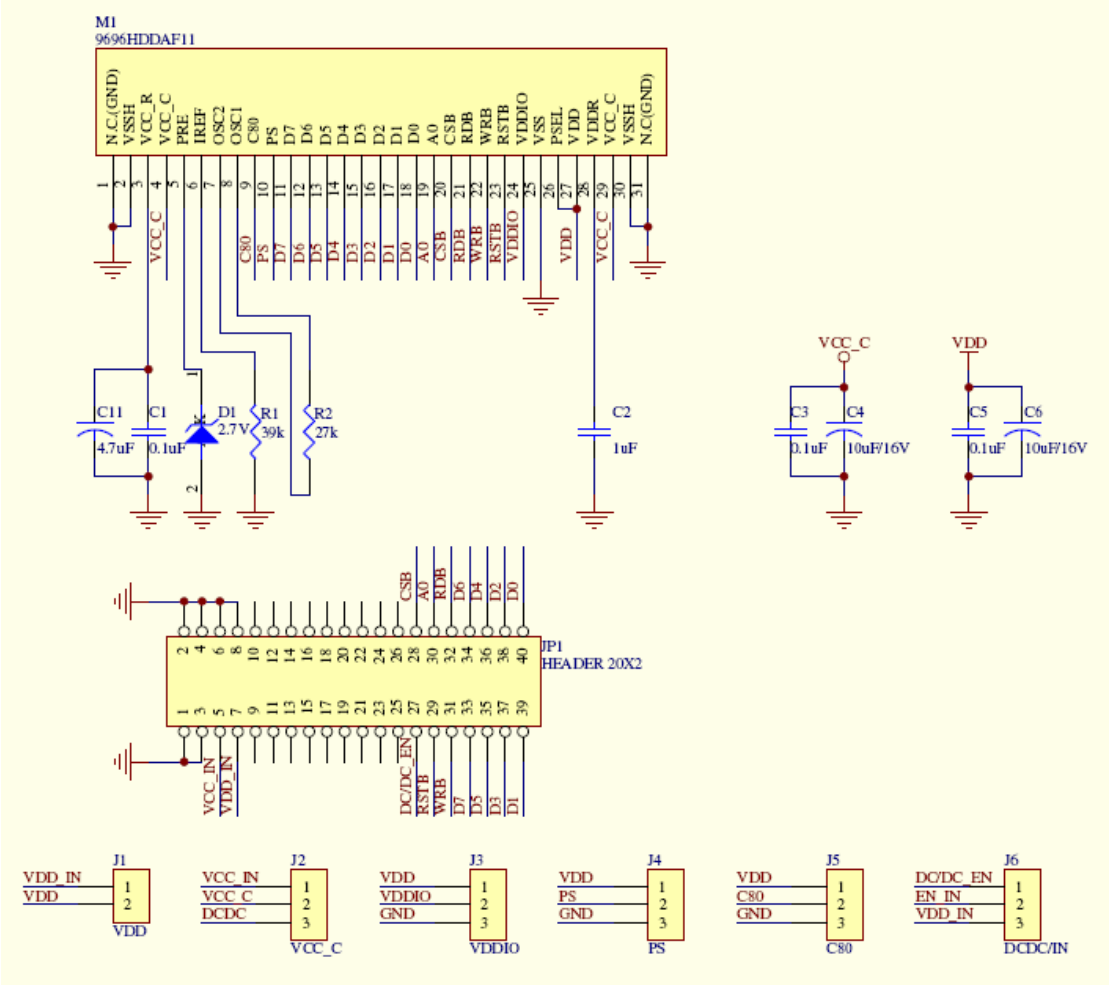
1.REVISION HISTORY

Date	Page	Contents	Version
200X/XX/XX		Preliminary	Preliminary 0.0

2.EVK Schematic



此版 **EVK** 上 **VDDIO** 外給功能已經內接 **VDD**，因此 J3 JUMP 不上件且無功能，待改版後才會有 VDDIO 外給功能

For this edition, VDDIO pin already accessed with VDD, so, it will cannot use external applicable function, and have no bond up with J3 JUMP component for this edition and J3 JUMP have no function in this edition, we will modify EVK in our next edition and recover function of external applicable for VDDIO.

3.Symbol define

D7-D0：These pins are 8-bit bi-directional data bus to be connected to the MCU's data bus.

The D0~D7 are for command and data inputs (8bit parallel interface).

CSB：This pin is the chip select input. The chip is enabled for MCU communication only when CS is pulled low.

RDB：When connecting to an 8080-microprocessor, this pin receives the Read (RD) signal. Data read operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin RD must be connected to VSS.

WRB：When 8080 interface mode is selected, this pin will be the Write (WR) input. Data write operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin R/W must be connected to VSS.

A0: This pin is Data/Command control pin. When the pin is pulled high, the data at D0-D7 is treated as display data. When the pin is pulled low, the data at D0-D7 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the timing characteristics diagrams at following pages and datasheet.

RESB：Reset SEPS114A(active low).

VCC：External Column Driving Power Supply.

VDD：Logic power supply.

GND：Power supply ground.

4.TIMMING CHARACTERISTICS

4.1 80-Series MPU parallel Interface

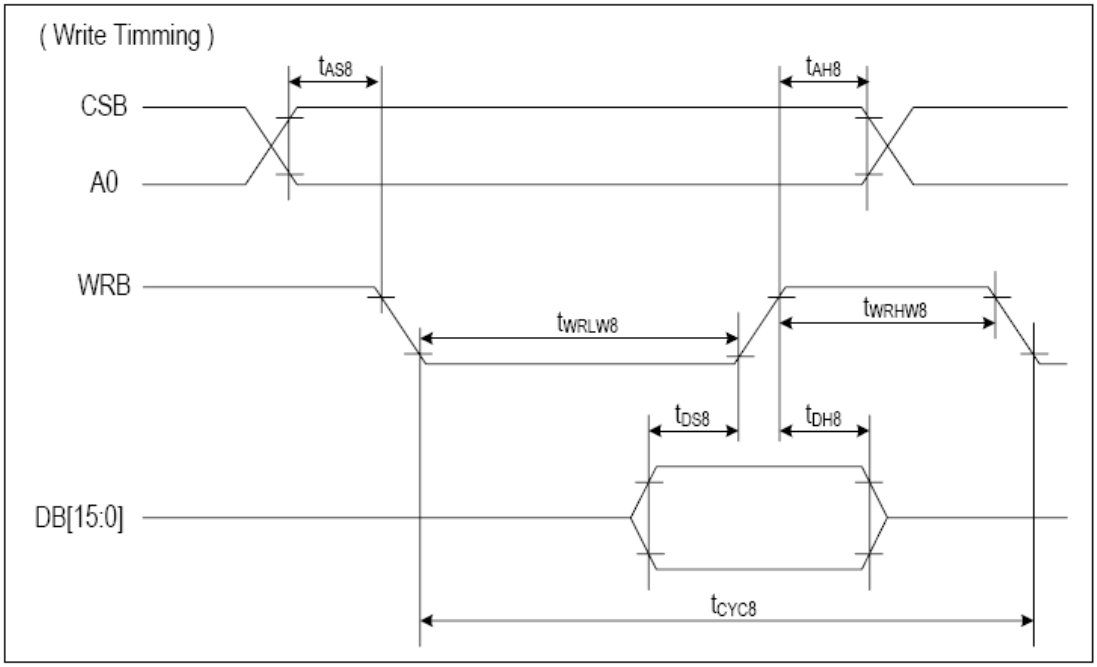


Figure 1 80-Series MPU parallel Interface Timing Diagram

(VDD = 2.8V, Ta = 25℃)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	t_{AH8}	-	5	-	ns	CSB
Address setup timing	t_{AS8}		5		ns	A0
System cycle timing	t_{CYC8}	-	100	-	ns	WRB
Write "L" pulse width	t_{WRLW8}		45		ns	
Write "H" pulse width	t_{WRHW8}		45		ns	
Data setup timing	t_{DS8}	-	30	-	ns	DB[15:0]
Data hold timing	t_{DH8}		10		ns	

notice) All the timing reference is 10% and 90% of VDDIO.

Table 1 80-Series MPU parallel Interface Timing Characteristics

4.2 6800-Series MPU parallel Interface

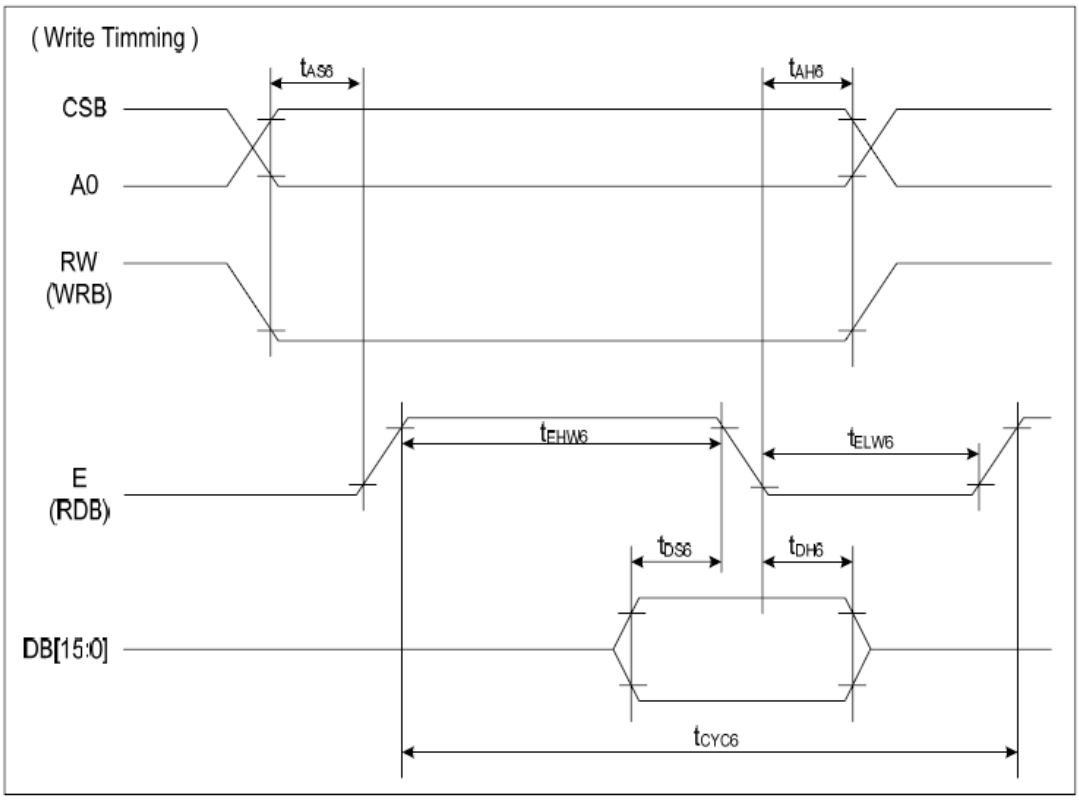


Figure 1 80-Series MPU parallel Interface Timing Diagram

(VDD = 2.8V, Ta = 25℃)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	t_{AH6}	-	5	-	ns	CSB
Address setup timing	t_{AS6}		5		ns	A0
System cycle timing	t_{CYC6}	-	100	-	ns	E
Write "L" pulse width	t_{ELW6}		45		ns	
Write "H" pulse width	t_{EHW6}		45		ns	
Data setup timing	t_{DS6}	-	40	-	ns	DB[15:0]
Data hold timing	t_{DH6}		10		ns	

Notice) All the timing reference is 10% and 90% of VDDIO.

Table 1 80-Series MPU parallel Interface Timing Characteristics

4.3 SPI(4-wire)-Series MPU parallel Interface

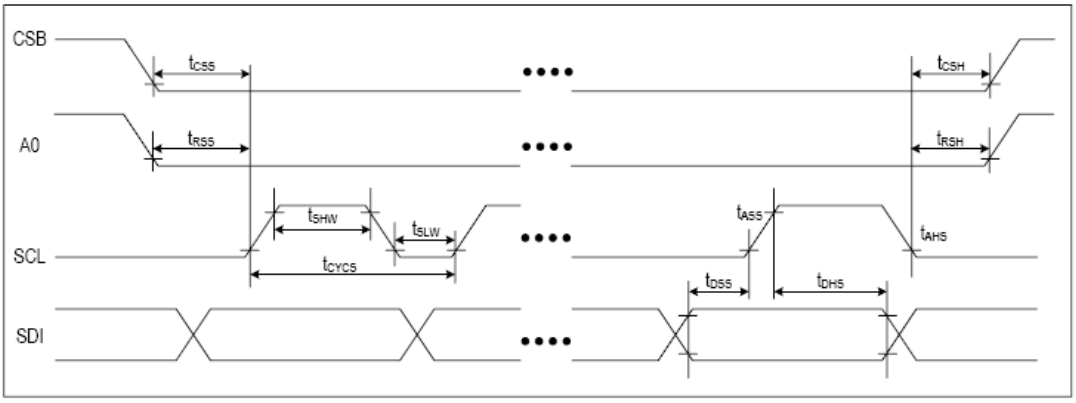


Figure 1 SPI(4-wire)-Series MPU parallel Interface Timing Diagram

(VDD = 2.8V, Ta = 25℃)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Serial clock cycle	t_{CYCS}	-	200	-	ns	SCL
SCL "H" pulse width	t_{SHW}		90		ns	
SCL "L" pulse width	t_{SLW}		90		ns	
Data setup timing	t_{DSS}	-	25	-	ns	SDI
Data hold timing	t_{DHS}		25		ns	
CSB-SCL timing	t_{CSS}	-	25	-	ns	CSB
CSB-hold timing	t_{CSH}		25		ns	
RS-SCL timing	T_{RSS}	-	25	-	ns	RS
RS-hold timing	T_{RSH}		25		ns	

Notice) All the timing reference is 10% and 90% of VDDIO.

Table 1 SPI(4-wire)-Series MPU parallel Interface Timing Characteristics

5.EVK use introduction

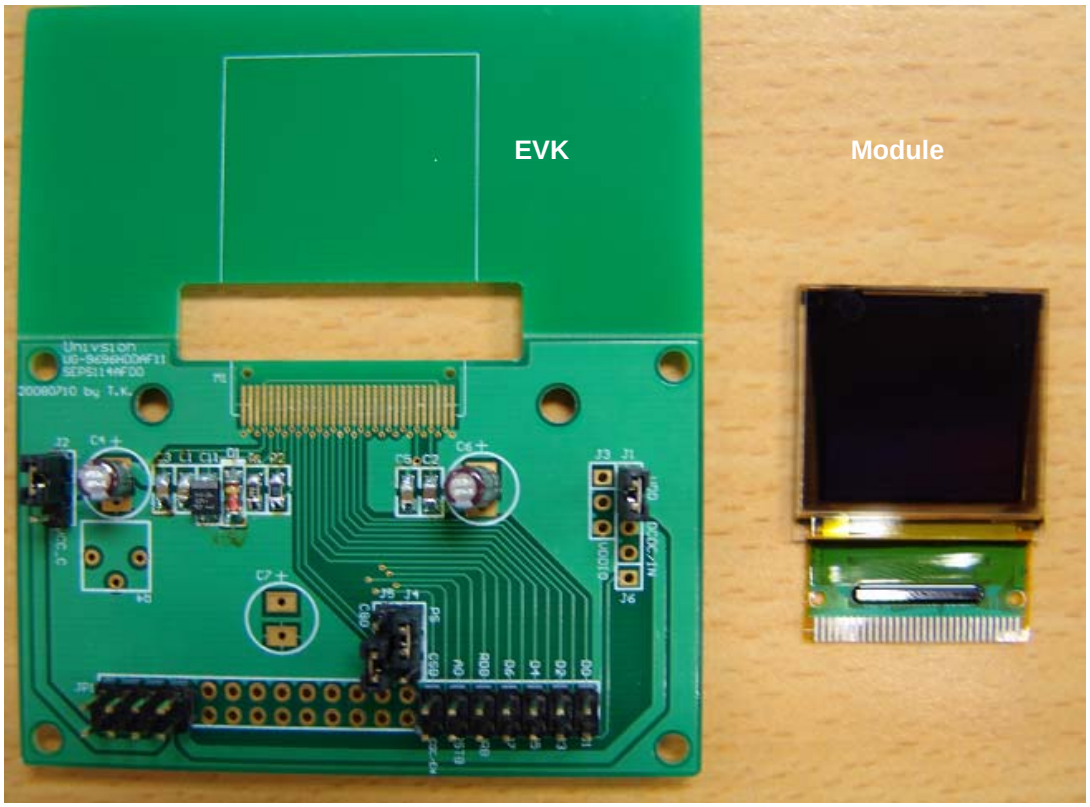


Figure 5 EVK PCB and OLED Module

UG-9696HDDAF11 is (COF) type module, please refer to Figure 5, Figure 6.User can use leading wire to connect EVK with customer's system. The example shows as Figure 7.

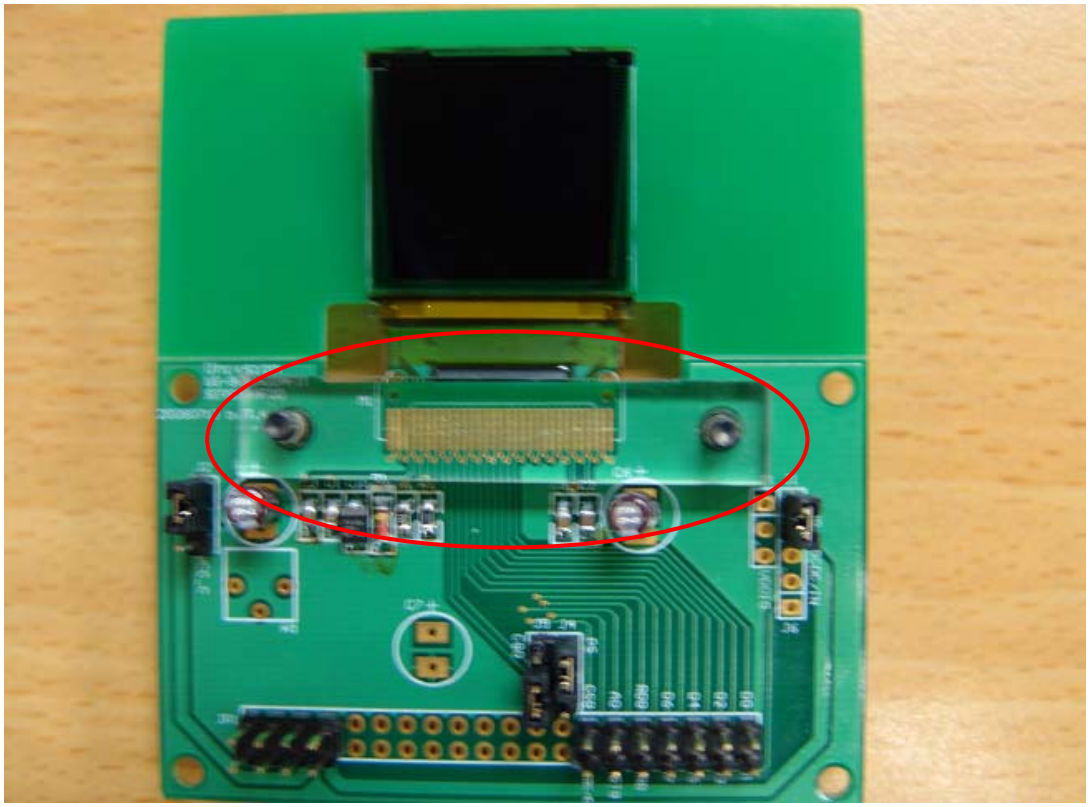


Figure 6 The combination of the module and EVK

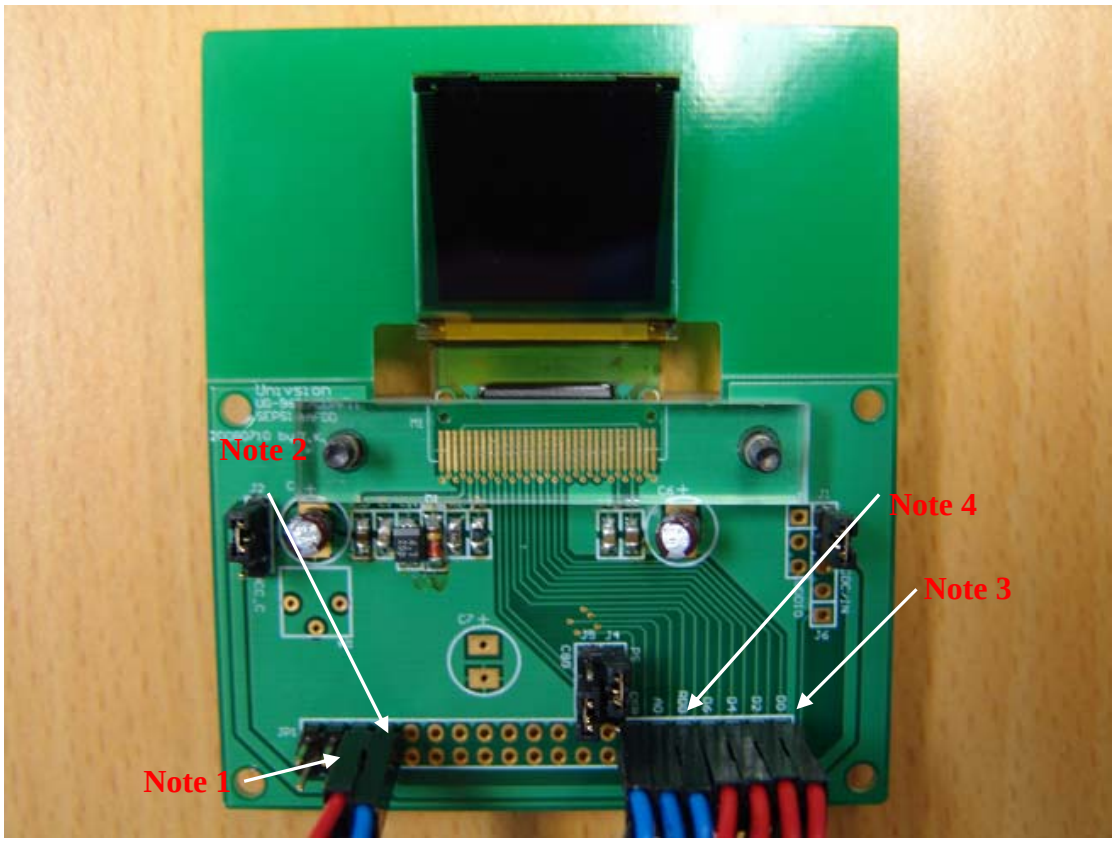


Figure 7 EVK with test platform

Note 1：It is OLED high voltage supply.

Note 2：It is logic voltage supply.

Note 3：Those are leading wire connect to control board. Those are data pin.(D0-D7)

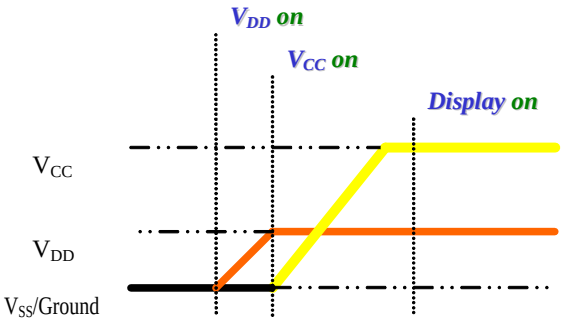
Note 4：Those are leading wire connect to control board. Those are control pin.
(RDB,WRB,A0,RSTB,CSB)

6.Power down and Power up Sequence

To protect OLED panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge up or discharge before/after operation.

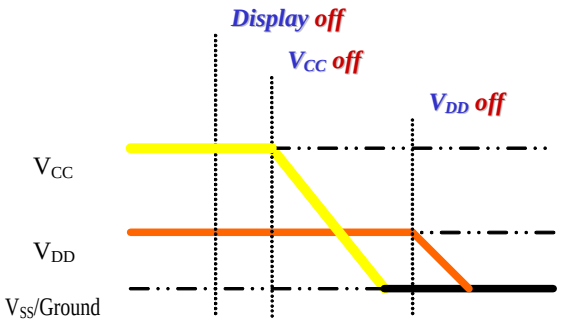
Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Driver IC Initial Setting
4. Clear Screen
5. Power up V_{DDH}
6. Delay 100ms
   (when V_{DD} is stable)
7. Send Display on command



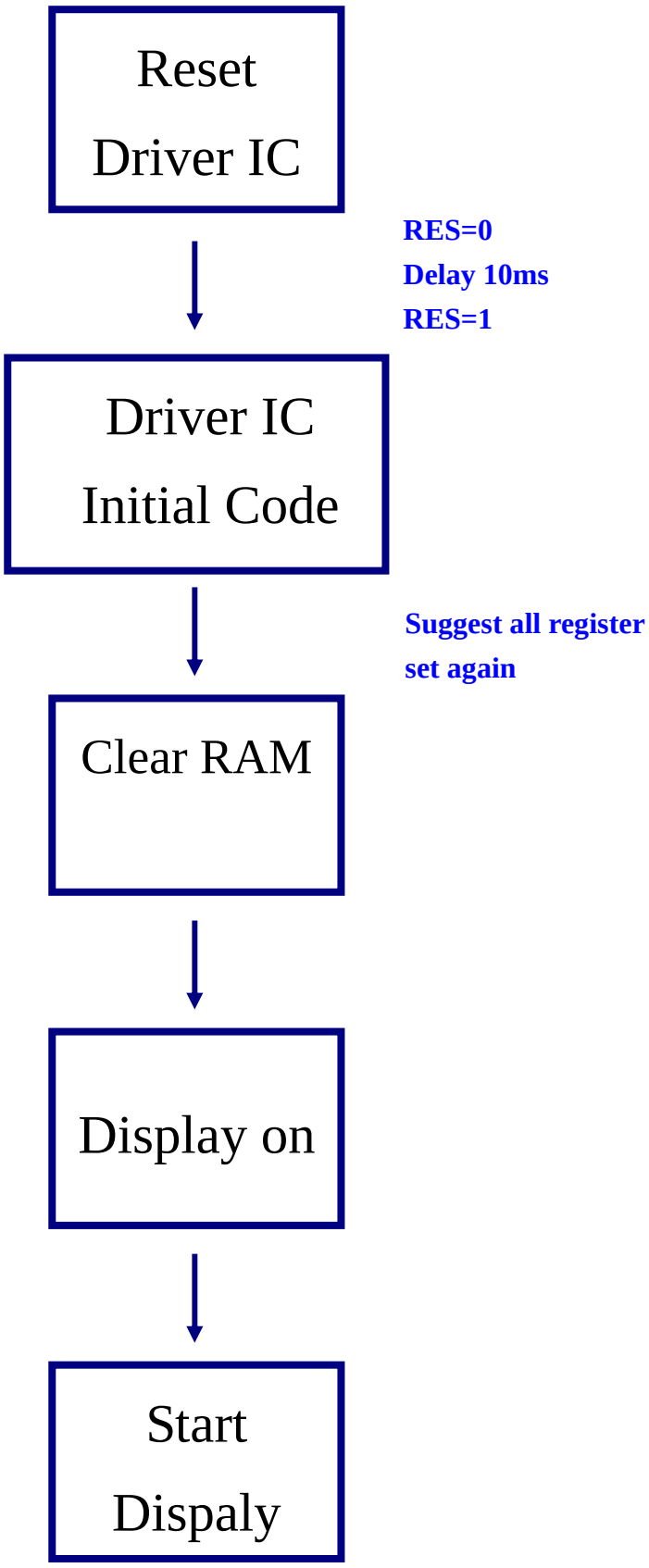
Power down Sequence:

1. Send Display off command
2. Power down V_{DDH}
3. Delay 100ms
   (when V_{DDH} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



7.How to use SEPS114A module

7.1 Initial Step Flow



7.2 RD recommend Initial Code for 80 Interface: